Chapter 1
Introduction
• **Architecture** = those attributes visible to the programmer
  – Instruction set, number of bits used for data representation, I/O mechanisms, addressing techniques.
  – e.g. Is there a multiply instruction?

• **Organization** = how features are implemented
  – Control signals, interfaces, memory technology.
  – e.g. Is there a hardware multiply unit or is it done by repeated addition?
The boundary between organization and architecture is not sharply defined, and it also changes in time:

- **Principle of Equivalence of Hardware and Software**
Decimal vs. Binary multipliers in the computer world

Zhang Zhilei (red) and Roberto Cammarelle (blue) fight at the Beijing Olympics (2008). (Photo credit: Al Bello/Getty Images)
## Decimal multipliers

<table>
<thead>
<tr>
<th>Prefix Symbol</th>
<th>1000(^m)</th>
<th>10(^n)</th>
<th>Decimal</th>
</tr>
</thead>
<tbody>
<tr>
<td>yotta (Y)</td>
<td>1000(^8)</td>
<td>10(^{24})</td>
<td>1,000,000,000,000,000,000,000,000,000,000</td>
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<tr>
<td>zetta (Z)</td>
<td>1000(^7)</td>
<td>10(^{21})</td>
<td>1,000,000,000,000,000,000,000,000,000,000</td>
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<tr>
<td>exa (E)</td>
<td>1000(^6)</td>
<td>10(^{18})</td>
<td>1,000,000,000,000,000,000,000,000,000,000</td>
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<tr>
<td>peta (P)</td>
<td>1000(^5)</td>
<td>10(^{15})</td>
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</tr>
<tr>
<td>tera (T)</td>
<td>1000(^4)</td>
<td>10(^{12})</td>
<td>1,000,000,000,000,000,000,000,000,000,000</td>
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<tr>
<td>giga (G)</td>
<td>1000(^3)</td>
<td>10(^9)</td>
<td>1,000,000,000,000,000,000,000,000,000,000</td>
</tr>
<tr>
<td>mega (M)</td>
<td>1000(^2)</td>
<td>10(^6)</td>
<td>1,000,000,000,000,000,000,000,000,000,000</td>
</tr>
<tr>
<td>kilo (k)</td>
<td>1000(^1)</td>
<td>10(^3)</td>
<td>1,000,000,000,000,000,000,000,000,000,000</td>
</tr>
<tr>
<td>hecto (h)</td>
<td>1000(^{2/3})</td>
<td>10(^2)</td>
<td>100,000,000,000,000,000,000,000,000,000,000</td>
</tr>
<tr>
<td>deca (da)</td>
<td>1000(^{1/3})</td>
<td>10(^1)</td>
<td>10,000,000,000,000,000,000,000,000,000,000</td>
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<table>
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<th>1000(^0)</th>
<th>10(^0)</th>
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<tbody>
<tr>
<td>deci (d)</td>
<td>1000(^{-1/3})</td>
<td>10(^{-1})</td>
</tr>
<tr>
<td>centi (c)</td>
<td>1000(^{-2/3})</td>
<td>10(^{-2})</td>
</tr>
<tr>
<td>milli (m)</td>
<td>1000(^{-1})</td>
<td>10(^{-3})</td>
</tr>
<tr>
<td>micro (µ)</td>
<td>1000(^{-2})</td>
<td>10(^{-6})</td>
</tr>
<tr>
<td>nano (n)</td>
<td>1000(^{-3})</td>
<td>10(^{-9})</td>
</tr>
<tr>
<td>pico (p)</td>
<td>1000(^{-4})</td>
<td>10(^{-12})</td>
</tr>
<tr>
<td>femto (f)</td>
<td>1000(^{-5})</td>
<td>10(^{-15})</td>
</tr>
<tr>
<td>atto (a)</td>
<td>1000(^{-6})</td>
<td>10(^{-18})</td>
</tr>
<tr>
<td>zepto (z)</td>
<td>1000(^{-7})</td>
<td>10(^{-21})</td>
</tr>
<tr>
<td>yocto (y)</td>
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<td>10(^{-24})</td>
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## Binary multipliers

<table>
<thead>
<tr>
<th>IEC prefix</th>
<th>Name</th>
<th>Symbol</th>
<th>Base 2</th>
<th>Base 1024</th>
<th>Value</th>
<th>Base 10</th>
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<tbody>
<tr>
<td>kibi</td>
<td>Ki</td>
<td>2^{10}</td>
<td>1024^1</td>
<td>1 024</td>
<td>1 024</td>
<td>1.02 × 10³</td>
</tr>
<tr>
<td>mebi</td>
<td>Mi</td>
<td>2^{20}</td>
<td>1024^2</td>
<td>1 048 576</td>
<td>1 048 576</td>
<td>1.05 × 10⁶</td>
</tr>
<tr>
<td>gibi</td>
<td>Gi</td>
<td>2^{30}</td>
<td>1024^3</td>
<td>1 073 741 824</td>
<td>1 073 741 824</td>
<td>1.07 × 10⁹</td>
</tr>
<tr>
<td>tebi</td>
<td>Ti</td>
<td>2^{40}</td>
<td>1024^4</td>
<td>1 099 511 627 776</td>
<td>1 099 511 627 776</td>
<td>1.10 × 10¹²</td>
</tr>
<tr>
<td>pebi</td>
<td>Pi</td>
<td>2^{50}</td>
<td>1024^5</td>
<td>1 125 899 906 842 624</td>
<td>1 125 899 906 842 624</td>
<td>1.13 × 10¹⁵</td>
</tr>
<tr>
<td>exbi</td>
<td>Ei</td>
<td>2^{60}</td>
<td>1024^6</td>
<td>1 152 921 504 606 846 976</td>
<td>1 152 921 504 606 846 976</td>
<td>1.15 × 10¹⁸</td>
</tr>
<tr>
<td>zebi</td>
<td>Zi</td>
<td>2^{70}</td>
<td>1024^7</td>
<td>1 180 591 620 717 411 303 424</td>
<td>1 180 591 620 717 411 303 424</td>
<td>1.18 × 10²¹</td>
</tr>
<tr>
<td>yobi</td>
<td>Yi</td>
<td>2^{80}</td>
<td>1024^8</td>
<td>1 208 925 819 614 629 174 706 176</td>
<td>1 208 925 819 614 629 174 706 176</td>
<td>1.21 × 10²⁴</td>
</tr>
</tbody>
</table>

Measurement units for computers: decimal vs. binary

Comparison of Decimal and Binary Units

Source: http://en.wikipedia.org/wiki/Binary_prefix
Prove that the difference between a tebibyte and a terabyte is 9.05%
Prove that the difference between a tebibyte and a terabyte is 9.05%

1 TiB = 1024^4 B = 1,099,511,627,776 B
1 TB = 1000^4 B = 1,000,000,000,000 B

(1 TiB – 1 TB)/1 TiB = 0.09050529
Further twist: physical vs. logical capacity

Up to 16% of drive capacity is lost in formatting.

Up to 25% of the link capacity can be lost in data transmission (TCP/IP over ATM) due to protocol overhead.
Cycle time is the reciprocal of clock frequency.

Example: A bus operating at 250 MHz has a cycle time of 4 nanoseconds:

\[
1 / (250,000,000 \text{ cycles/second}) = 4 \text{ ns/cycle}
\]
A computer’s bus is operating at 133 MHz. What is the duration of one cycle?
A computer’s bus is operating at 133MHz. What is the duration of one cycle?

1/ (133,000,000 cycles/second) = 0.00000000752 second/cycle = 7.52 ns/cycle
A computer’s hard-disk rotates at 7200 RPM. What is the average delay when accessing a sector on this disk?
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What is the average delay when accessing a sector on this disk?

RPM = rotations per minute

7200 RPM = 7200 / 60 = 120 RPS

1 full rotation takes …
A computer’s hard-disk rotates at 7200 RPM.

What is the average delay when accessing a sector on this disk?

RPM = rotations per minute

7200 RPM = 7200 / 60 = 120 RPS

1 full rotation takes $1/120 = 8.3$ ms

On average, the disk has to perform half a rotation $→ 4.17$ ms
A computer’s hard-disk is labeled "1.5 TB".

Assuming the manufacturer meant the decimal "tera", how many bytes are there on the disk? Call this capacity $C_{10}$.

Assuming the manufacturer meant "tera-binary", how many bytes are there on the disk? Call this capacity $C_2$.

Which is greater, $C_2$ or $C_{10}$?
A computer’s hard-disk is labeled "1.5 TB"

Taking $C_{10}$ as our starting point, by what percentage is $C_2$ greater than $C_{10}$?
Read and take notes in notebook for next time:
Section 1.3 An Example System

What does it all mean??
It is estimated that the NSA (National Security Agency) collects roughly ___________ GB of data every hour.

Hint: See p.6 of our text.

Hoe much data does the NSA collect in a year? (Use the appropriate multiplier)
It is estimated that the NSA (National Security Agency) collects roughly 2 million GB of data every hour.

How much data does the NSA collect in a year? (Use the appropriate multiplier)

\[2,000,000 \times 24 \times 365 = 17,520,000,000 \text{ GB} \approx 17.5 \text{ EB}\]
Explain the difference between the system bus and I/O bus.

What is the most popular I/O bus standard today?

Hint: See p.12 of our text.
QUIZ

Explain the difference between the system bus and I/O bus:

• System bus connects CPU, Memory, and standard peripherals, such as HDD, DVD, etc.
• I/O bus augments the system bus by connecting other peripherals (incl. today video cards)

What is the most popular I/O bus standard today? PCIe
1.3 An Example System

Two important questions:

What assurance do we have that

• Each computer component will operate as we expect?

• Computer components will operate together as we expect?
1.4 Standards Organizations

- The Institute of Electrical and Electronic Engineers (IEEE)
- The International Telecommunications Union (ITU)
- National groups:
  - The American National Standards Institute (ANSI)
  - The British Standards Institution (BSI)
- The International Organization for Standardization (ISO)

Note: ISO is not just an acronym. It comes from the Greek isos, meaning “equal.”
1.5 Historical Development

**Generation Zero: Mechanical** Calculating Machines (1642 - 1945)
- Calculating Clock - Wilhelm Schickard (1623).
- Pascaline - Blaise Pascal (1642).
- Stepped Reckoner – Gotfried Leibniz (1672)
- Programmable loom - Joseph Jacquard (1801)
- Difference Engine - Charles Babbage (1822 - 1835); he also designed but never built the Analytical Engine.
- Punched card tabulating machines - Herman Hollerith (1889). 

  Hollerith cards were commonly used for computer input well into the 1970s!

- The "Bombe" at Bletchley Park (1942)
1.5 Historical Development

The **First Generation: Vacuum Tube** Computers (1945 - 1953)

- **Atanasoff -Berry Computer** (1937 - 1938) solved systems of linear equations.
  - John Atanasoff and Clifford Berry of Iowa State University.

- **Electronic Numerical Integrator and Computer (ENIAC)**
  - John Mauchly and J. Presper Eckert, University of Pennsylvania, 1946
  - Considered the first general-purpose electronic computer
1.5 Historical Development

• The **Second Generation: Transistorized Computers (1954 - 1965)**
  
  – IBM 7094 (scientific) and 1401 (business)
  – Digital Equipment Corporation (DEC) PDP-1
  – Univac 1100
  – Control Data Corporation 1604.
  – ... and many others.

These systems had few architectural similarities.
1.5 Historical Development

• The **Third Generation: Integrated Circuit** Computers (1965 - 1980)
  – IBM 360
  – DEC PDP-8 and PDP-11
  – Cray-1 supercomputer
  – . . . and many others.

• By this time, IBM had gained overwhelming dominance in the industry.
  – Computer manufacturers of this era were characterized as IBM and the BUNCH (Burroughs, Unisys, NCR, Control Data, and Honeywell).
1.5 Historical Development

The **Fourth Generation: VLSI** Computers

(1980 - ????)

– Very large scale integrated circuits (VLSI) have more than 10,000 components per chip.
– Enabled the creation of microprocessors.
– The first was the 4-bit **Intel 4004**.
– Later versions, such as the 8080, 8086, and 8088 spawned the idea of “personal computing.”
Fifth Generation Hardware (2001-today)

Multi-core processors
IBM Power4, released in 2001, had 2 cores in the same chip.

Not everyone agrees on what 5G means 😊
1.5 Historical Development

• Moore’s Law (1965)
  – Gordon Moore, Intel founder
  – “The density of transistors in an integrated circuit will double every year.”

• Contemporary version:
  – “The density of silicon chips doubles every 18 months.”

But this “law” cannot hold forever ...
Moore’s Law:
Shrinking logic gate size

Current gate-based transistor architectures will have to stop at 5nm-wide Gates b/c of quantum tunnelling.
1.5 Historical Development

• Rock’s Law

– Arthur Rock, Intel financier

– “The cost of capital equipment to build semiconductors will double every four years.”

– In 1968, a new chip plant cost about $12,000.

At the time, $12,000 would buy a nice home in the suburbs.
An executive earning $12,000 per year was “making a very comfortable living.”
1.5 Historical Development

• Rock’s Law
  – In 2010, a chip plants under construction cost well over $4 billion.

    $4 billion is more than the gross domestic product of some small countries, like Barbados, Mauritania, and Rwanda!

  – For Moore’s Law to hold, Rock’s Law must fall, or vice versa. But no one can say which will give out first.
1.6 The Computer Level Hierarchy

- Each virtual machine layer is an abstraction of the level below it.
- The machines at each level execute their own particular instructions, calling upon machines at lower levels to perform tasks as required.
- Computer circuits ultimately carry out the work.
1.7 The von Neumann Model

• On the ENIAC, all programming was done at the digital logic level.

• Programming the computer involved moving plugs and wires.

• A different hardware configuration was needed to solve every unique problem type.

Configuring the ENIAC to solve a “simple” problem required many days labor by skilled technicians.
• Inventors of the ENIAC, John Mauchley and J. Presper Eckert, conceived of a computer that could store instructions in memory.

• The invention of this idea has since been ascribed to a mathematician, John von Neumann, who was a contemporary of Mauchley and Eckert.

• Stored-program computers have become known as von Neumann Architecture systems.
Today’s \textbf{vN} computers have the following characteristics:

- Three hardware systems:
  - A central processing unit (CPU)
  - A main memory system
  - An I/O system

- The capacity to carry out sequential instruction processing.

- A single data path between the CPU and main memory.
  - This single path is known as the \textit{von Neumann bottleneck}. 
vN computers employ a fetch-get-decode-execute cycle to run programs as follows . . .
• The control unit fetches the next instruction from memory using the program counter to determine where the instruction is located.
• The instruction is decoded into a language that the ALU can understand.
• Any data operands required to execute the instruction are gotten from memory and placed into registers within the CPU.
• The ALU executes the instruction and places results in registers or memory.
Conventional stored-program computers have undergone many incremental improvements over the years. These improvements include adding specialized buses, floating-point units, and cache memories, to name only a few. But enormous improvements in computational power require departure from the classic von Neumann architecture. Adding processors is one approach → multi-processor
In the late 1960s, high-performance computer systems were equipped with dual processors to increase computational throughput.

In the 1970s supercomputer systems were introduced with 32 processors.

Supercomputers with 1,000 processors were built in the 1980s.

In 1999, IBM announced its Blue Gene system containing over 1 million processors.
1.8 Non-von Neumann Models

• **Multicore** architectures have multiple CPUs on a single chip.

• Dual-core and quad-core chips are commonplace in desktop systems.

• Multi-core systems provide the ability to multitask
  – E.g., browse the Web while burning a CD

• Multithreaded applications spread mini-processes, *threads*, across one or more processors for increased throughput.
Read the entire Ch.1 and take notes in notebook!
Homework for Ch.1

End of chapter exercises 2, 9, 14, 22

Due next Thursday at the beginning of class